

Application No.: 10/646,406

Docket No.: JCLA10428

**In The Abstract:**

Please amend the abstract as follows:

~~The embodiment of the~~The present invention provides a joint clock source coupling architecture of a time division duplex (TDD) transceiver to minimize a circuit element interference and stabilize a performance of a circuit element within the TDD transceiver and a method thereof. Thereby, a communication link of the TDD transceiver is ensured, and a throughput of the TDD transceiver is increased. The method used to construct the architecture includes: providing a medium; constructing an analog circuit and a digital circuit; constructing an analog-to-digital (A/D) interface and a digital-to-analog (D/A) interface; providing a first ground reference and a second ground reference; providing a joint clock source for supplying clock pulses to the analog circuit, the digital circuit, the A/D interface, and the D/A interface; and connecting a ground reference of the joint clock source directly to the first ground reference.